PI3HDMI301

PI3HDMI301 HDMI-HDMI Demo Board Rev.B User Manual

by Ada Yip

Introduction

This user manual describes the components and the usage of PI3HDMI301 HDMI-HDMI Demo Board Rev.B. HDMI connectors are used as input and output connectors for the following HDMI-HDMI demo board version.

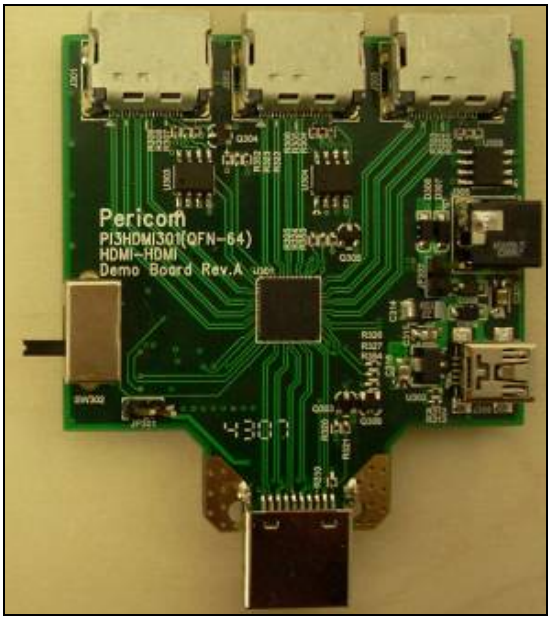


Figure 1a: Top View of PI3HDMI301 HDMI-HDMI Demo Board

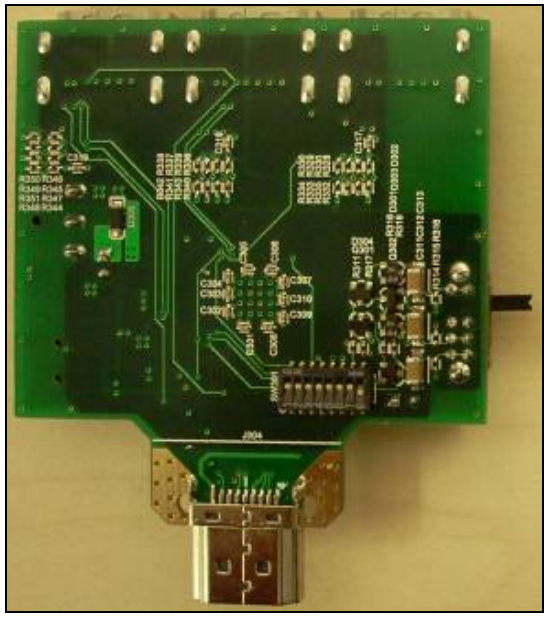


Figure 1b: Bottom View of PI3HDMI301 HDMI-HDMI Demo Board

Key Components / Circuits

a. 5V of PI3HDMI301 demo board can be supplied via three ways, i.e. using 5V supplied from Input Port, Power Jack, or from USB Type B Connector. Jumper JP302 on demo board is not connected at default. If using voltage of input port to power up the entire board, jumper must be added.

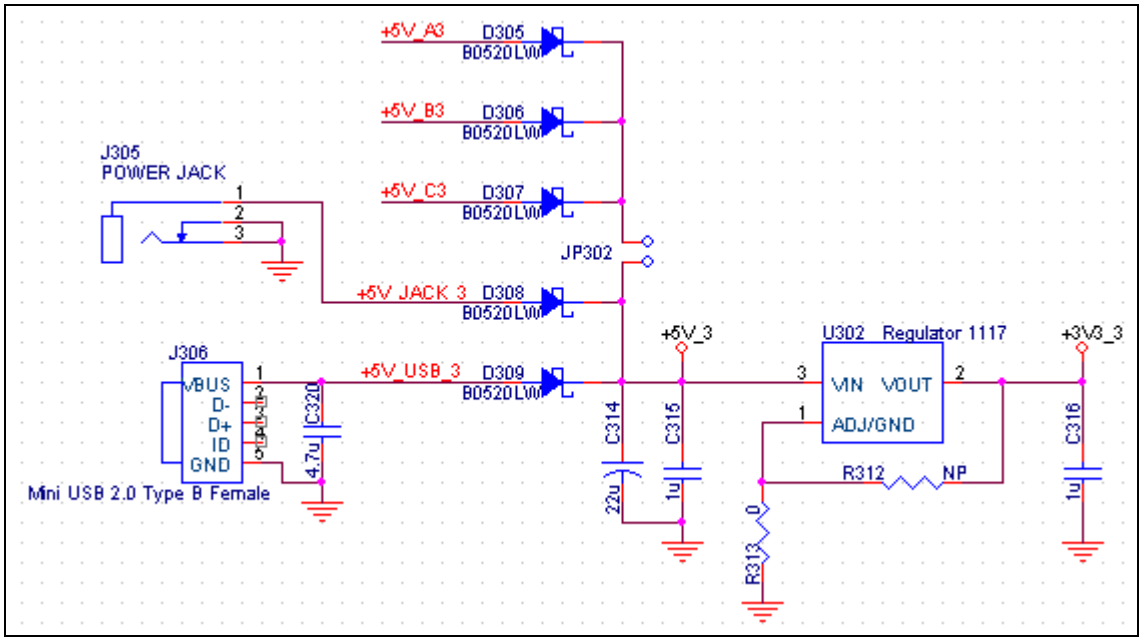


Figure 2: Schematic of 5V Power Supply of PI3HDMI301 HDMI-HDMI Demo Board Rev.B

5V supplying to output HDMI connector is provided by +5V_3 power via shorting Jumper JP301.

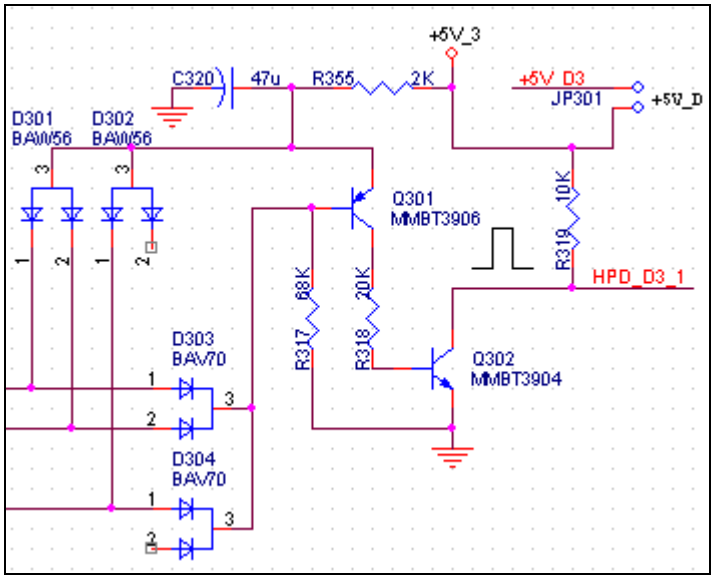


Figure 3: Schematic of 5V Power Supply to Output HDMI Connector

b. An HPD pulse of 250ms is generated at HPD_D3_1 pin when switching port via switch SW302 in the following circuit. This pulse is sent back to HPD_SINK pin of PI3HDMI301 to introduce an HPD reset signal.

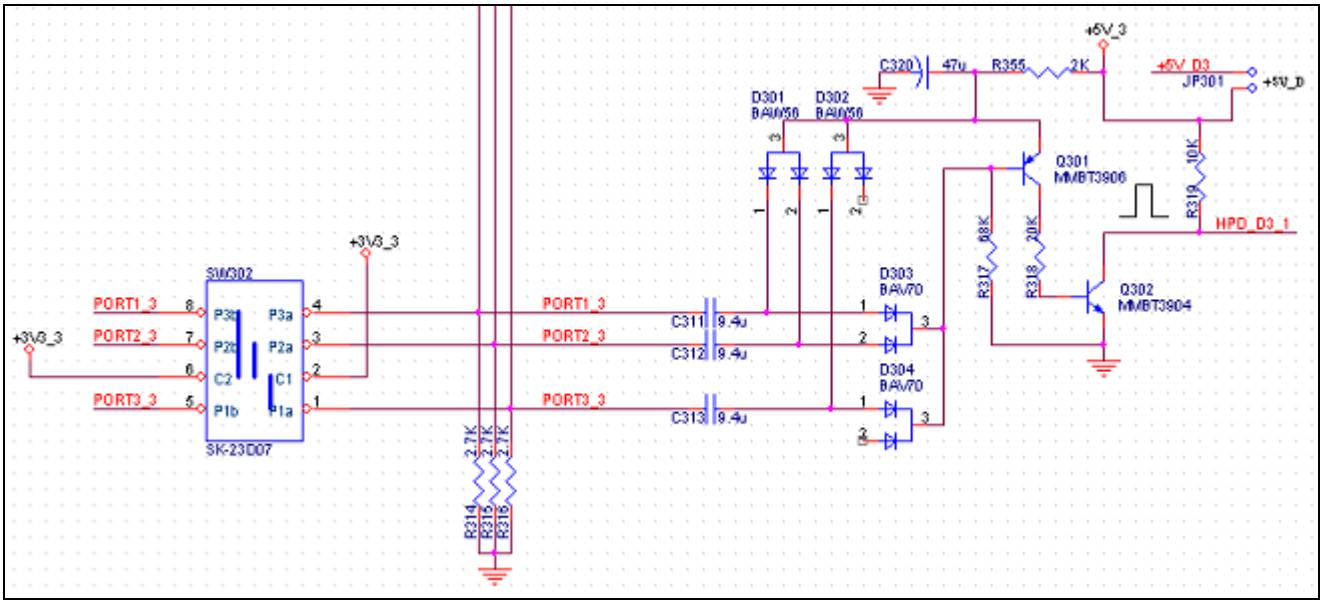


Figure 4: HPD Reset Pulse Circuit

The pulse will be sent to the HPD pin of one selected port among three, HPD_A3_1, HPD_B3_1 or HPD_C3_1. This pulse will then initiate a reset of HPD at input connector side, HPD_A3, HPD_B3 or HPD_C3, through NPN transistor, Q304, Q305 or Q306, respectively. Please refer to Figure 5. Resetting HPD is to ensure that HDCP Transmitter Link State is reset back to reset state H0. For details, please refer to Application Note AN202.

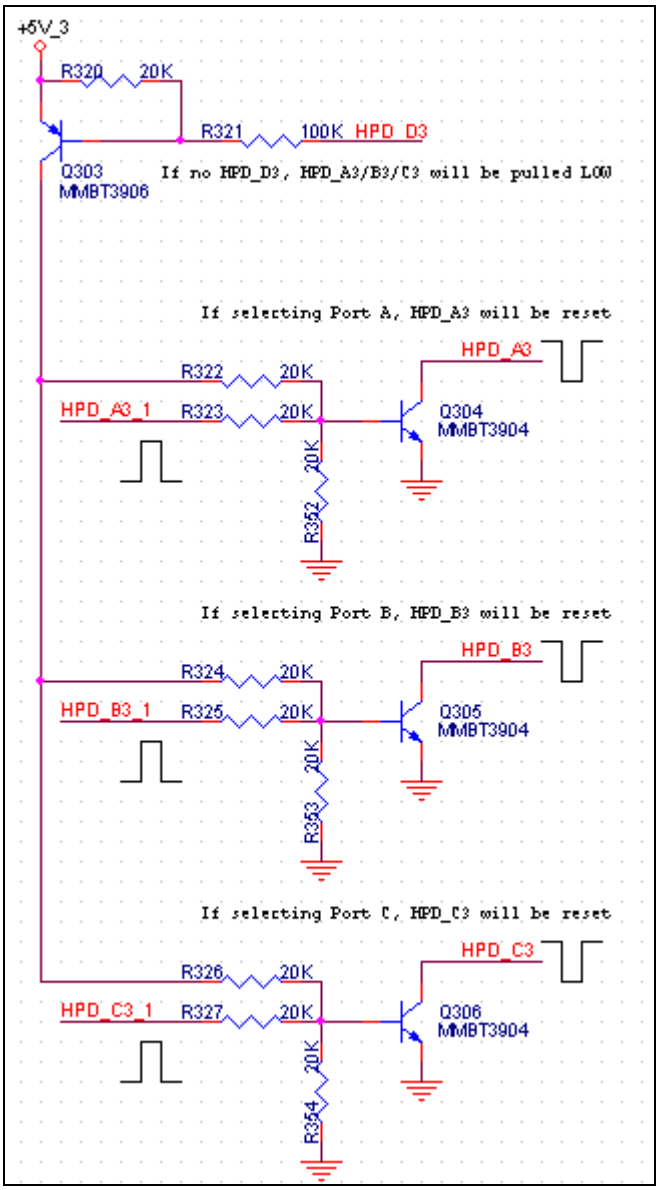


Figure 5: Source HPD Reset of PI3HDMI301 HDMI-HDMI Demo Board Rev.B

c. If Sink receiver is not connected to HDMI connector J304, HPD_D3 pin will become low. This will turn on PNP transistor Q303 and then three NPN transistors Q304, Q305 and Q306 in Figure 5. As a result, all the HPD signals at source side are pulled low and reset to state H0.

d. As PI3HDMI301 is a 3:1 MUX, a DP3T switch at reference SW302 is used to choose PORT1_3, PORT2_3 or PORT3_3 as the input port manually.

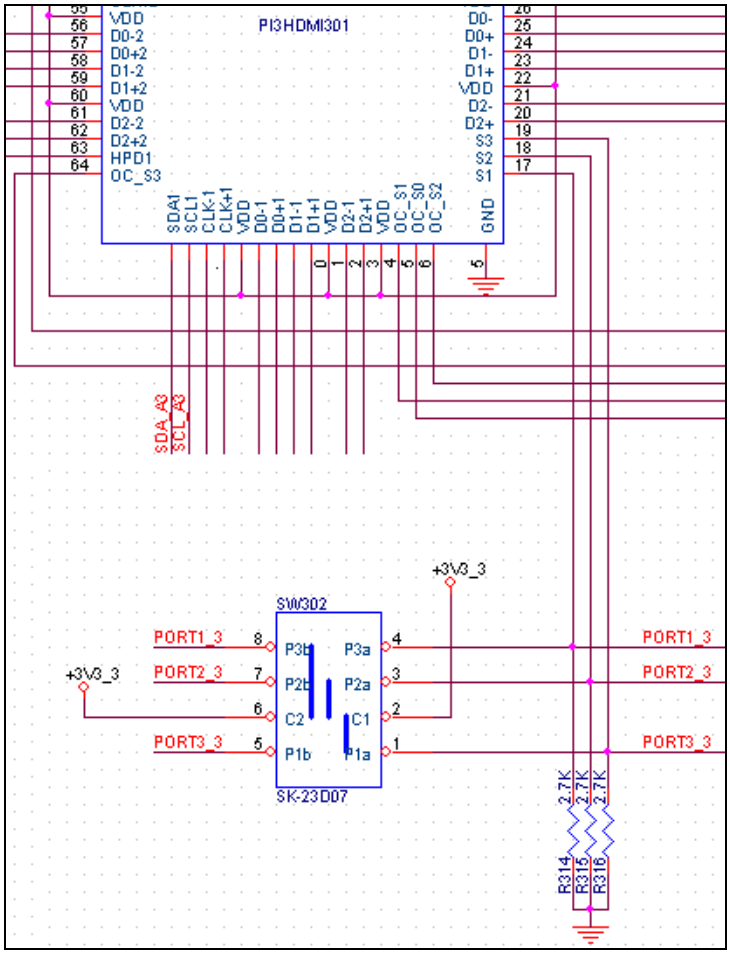


Figure 6: Schematic of Port Selection

Below shows the picture of a DP3T switch, SW302, which is located on the side of the demo board. The following is the operation:

1. When switch SW302 is switched up, output port J304 is connected to PORT3_3.
2. When the switch is in the middle, output port J304 is connected to PORT2_3.
3. When the switch is switched down, output port J304 is connected to PORT1_3.

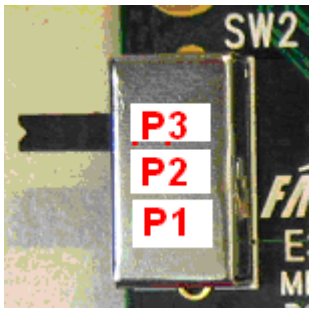


Figure 7: DP3T Switch SW302

e. Output Swing, De-emphasis and Equalization of signals can be adjusted by setting EQ_S[1:0] and OC_S[3:0] pins through switch SW301. These few control pins have internal pull-ups. Enable pin, /OE, can also be set using SW301. To enable the outputs of PI3HDMI301, /OE has to be shorted to ground.

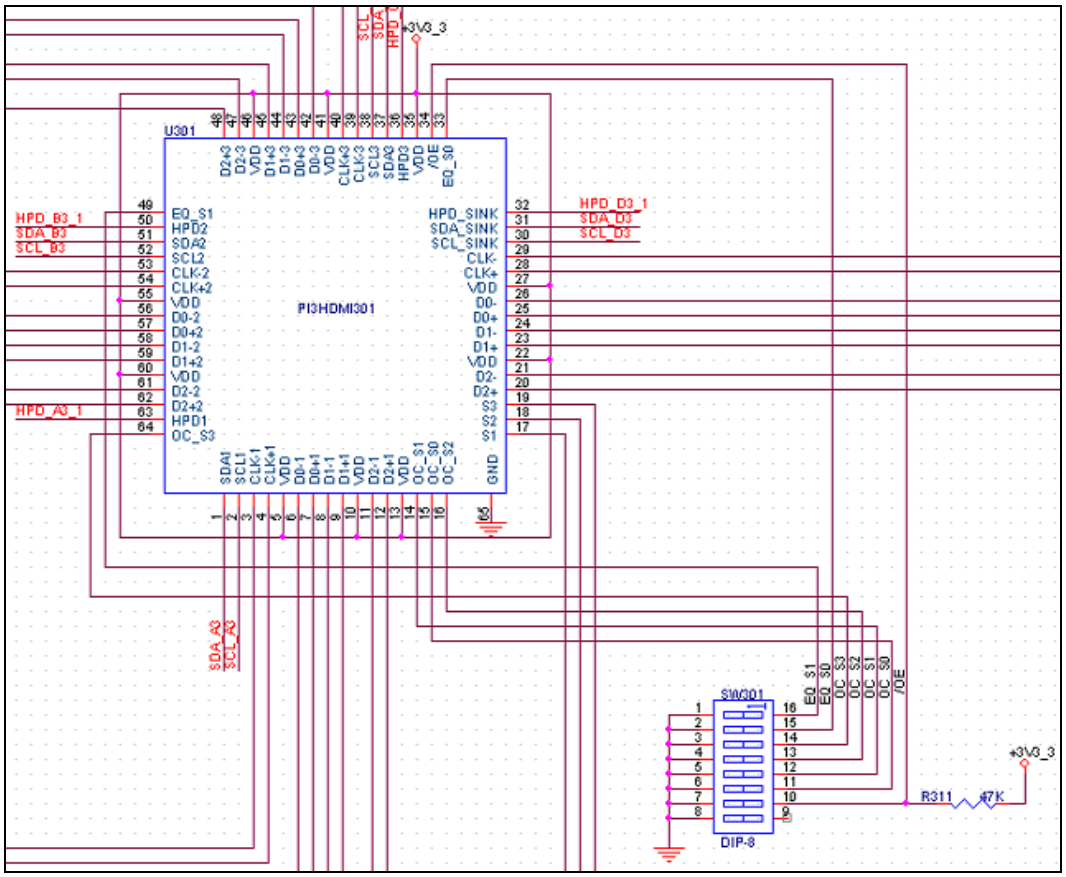


Figure 8: Control Pins of PI3HDMI301 HDMI-HDMI Demo Board Rev.B

f. Three AT24C02B EEPROMs are implemented in PI3HDMI301 demo board to model I2C application. The EEPROM is for DDC line capacitance measurement purpose. Please refer to p.18 for measurement result. A0 and A1 address inputs of each AT24C02B are pulled to low by external pull-down resistors while address A2 is pulled high. Write protection of each EEPROM is disabled.

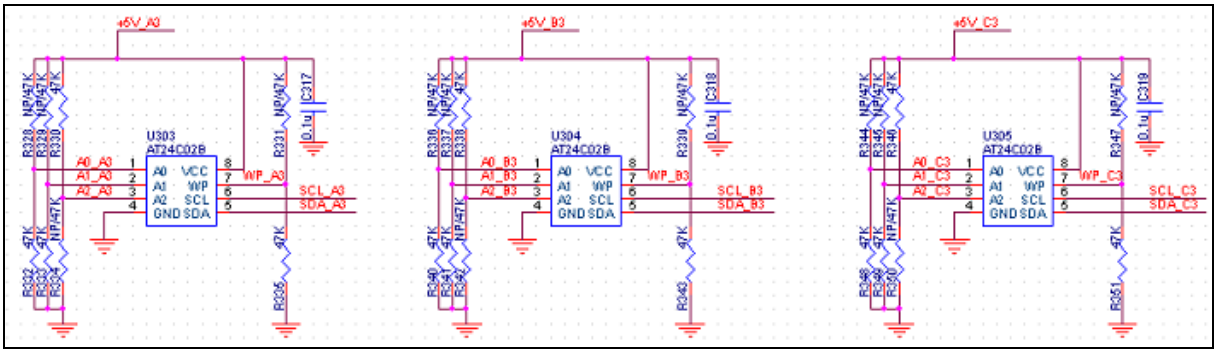


Figure 9: Schematic of EEPROM of PI3HDMI301 HDMI-HDMI Demo Board Rev.B

g. When source chipset does not generate CLK signal, noise may pass through an active PI3HDMI301 to cause output oscillation. To implement fail-safe feature to prevent from output oscillation, the input CLK is recommended to be biased externally. 100mV DC bias can be added to CLK+ by adding a 1.5kΩ pull-down resistor. To maintain trace impedance consistency, it is recommended to avoid stub between pull-down resistor pad and CLK signal trace on PCB layout.

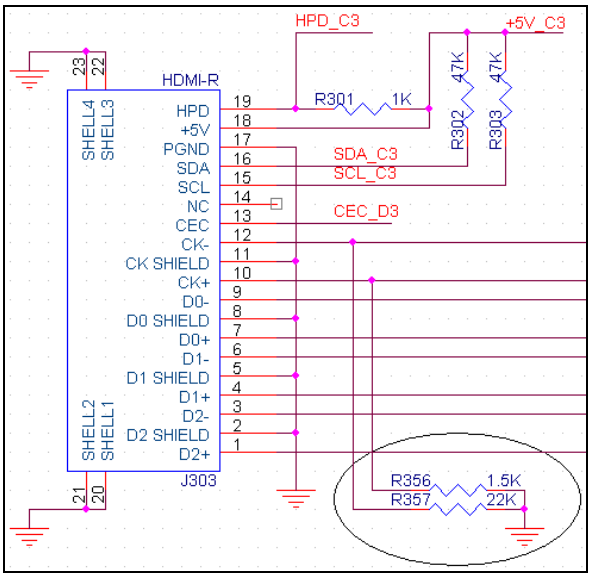


Figure 10: Input CLK External Pull-down of PI3HDMI301 HDMI-HDMI Demo Board Rev.B

In some DVD players, no sink current circuitry is implemented in TMDS. When these DVD players are de-selected, CLK signals stay at high level. To ensure the DVD players can enter idle mode when being de-selected, input CLK+/- pins are pulled down externally. By keeping 1.5kΩ pull-down resistor at CLK+ unchanged, another 22kΩ resistor is added to CLK- to pull CLK to low level when there is no 50Ω termination. HDCP can then be reset by RxSense when the port is being selected back.

Test Results

Few Source and Sink pre-test items are performed below. Source pre-test results with two output settings of swing and pre-/de-emphasis are tabulated. These two settings can generate passing eye diagrams with 1-meter cables connecting to both input and output connectors. All the eye diagrams of 13 different output settings are attached in section (d) below for reference.

a. Source Test ID 7-4: TMDS – Rise Time or Fall Time at 3dB Equalization & 1920x1080i Resolution

OC_S[3:0]	Output	T_{RISE}	T_{FALL}	Min Spec	Units
0000	CLK+/-	117.01	113.62	75	ps
	D2+/-	111.18	112.21	75	ps
0101	CLK+/-	108.74	102.91	75	ps
	D2+/-	104.69	106.89	75	ps

Table 1: Rise/Fall Times of TMDS at J304 when EQ=3dB and Resolution=1920x1080i

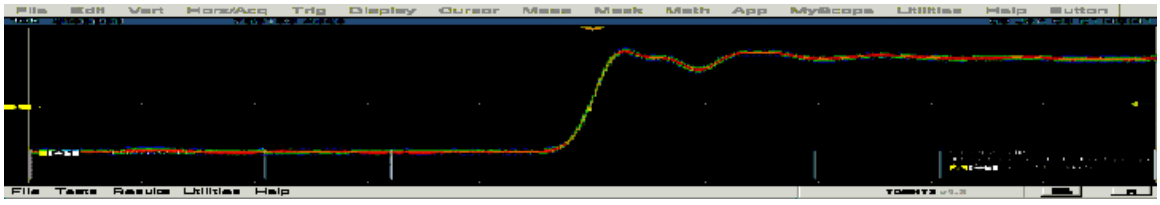


Figure 11a: T_{RISE} of CLK when OC_S[3:0]=0000, EQ=3dB and Resolution=1920x1080i

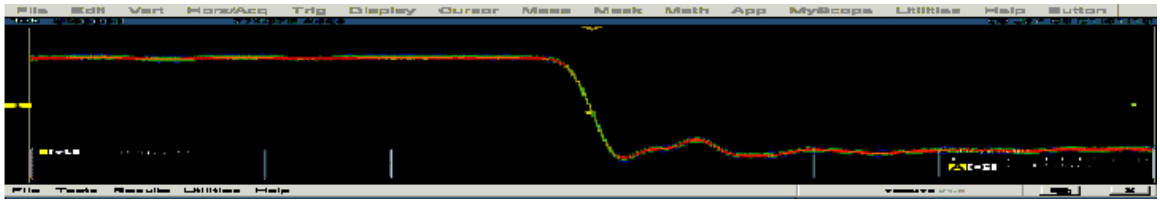


Figure 11b: T_{FALL} of CLK when OC_S[3:0]=0000, EQ=3dB and Resolution=1920x1080i

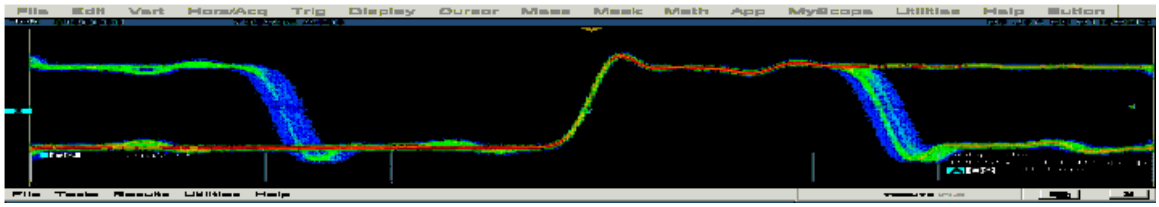


Figure 11c: T_{RISE} of D2 when OC_S[3:0]=0000, EQ=3dB and Resolution=1920x1080i

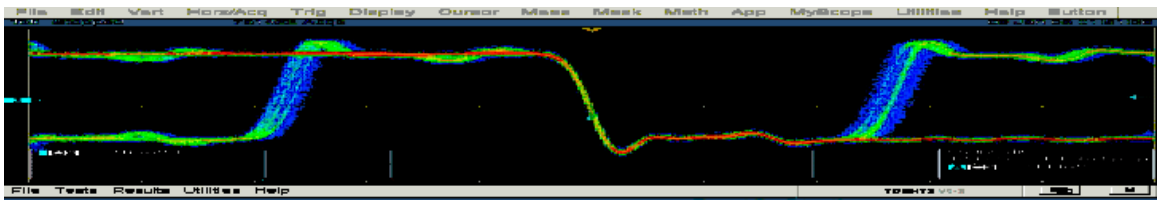


Figure 11d: T_{FALL} of D2 when OC_S[3:0]=0000, EQ=3dB and Resolution=1920x1080i

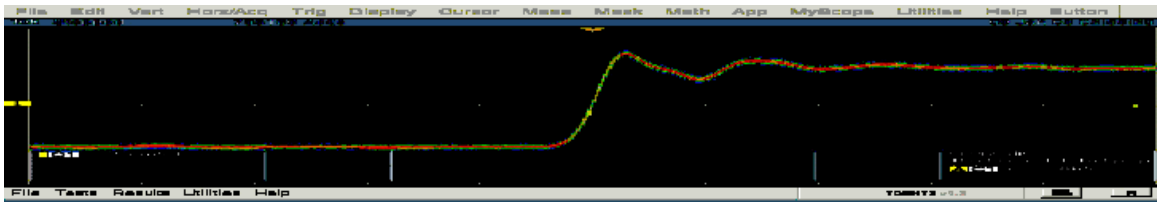


Figure 12a: T_{RISE} of CLK when OC_S[3:0]=0101, EQ=3dB and Resolution=1920x1080i

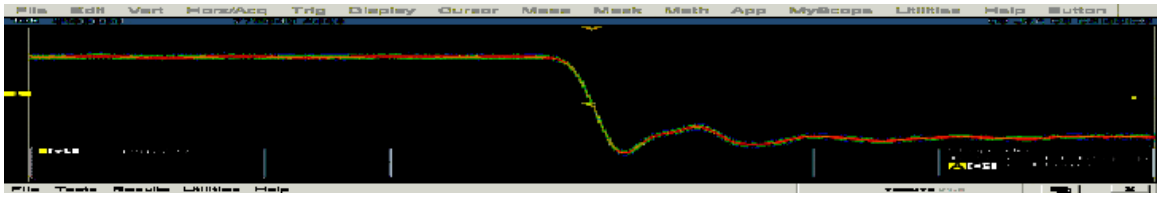


Figure 12b: T_{FALL} of CLK when OC_S[3:0]=0101, EQ=3dB and Resolution=1920x1080i

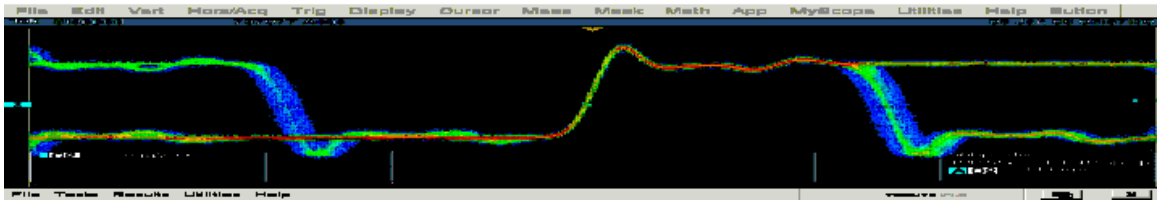


Figure 12c: T_{RISE} of D2 when OC_S[3:0]=0101, EQ=3dB and Resolution=1920x1080i

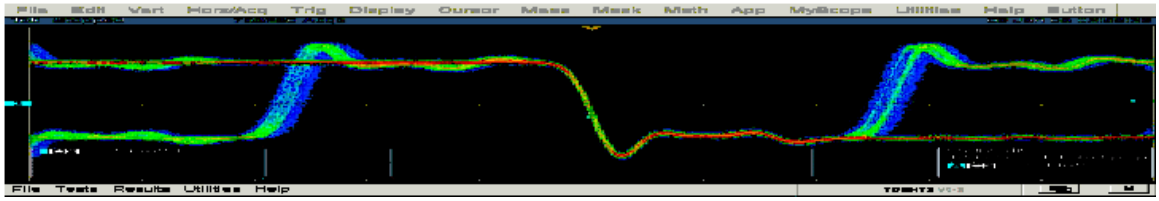


Figure 12d: T_{FALL} of D2 when OC_S[3:0]=0101, EQ=3dB and Resolution=1920x1080i

b. Source Test ID 7-8: TMDS – Clock Duty Cycle at 3dB Equalization & 1920x1080i Resolution

Output	Min Duty Cycle	Max Duty Cycle	Min Spec	Max Spec	Units
CLK+/-	49.00	50.49	40	60	%

Table 2: Clock Duty Cycle at J304 when EQ=3dB and Resolution=1920x1080i

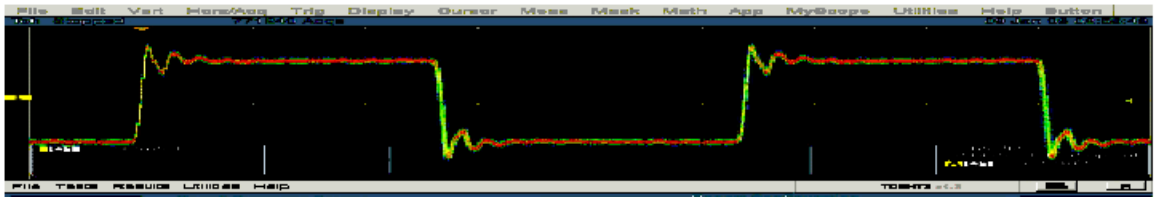


Figure 13a: Max Duty Cycle of CLK when EQ=3dB and Resolution=1920x1080i

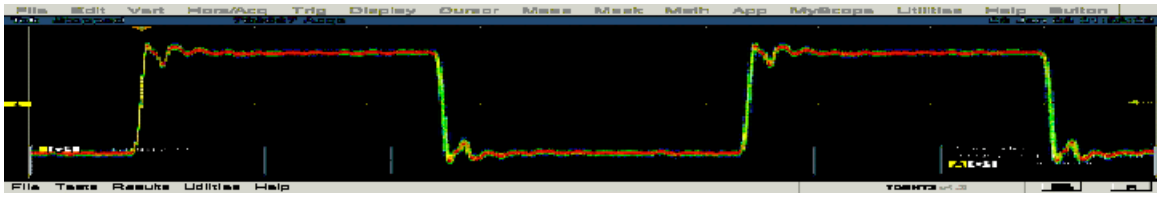


Figure 13b: Min Duty Cycle of CLK when EQ=3dB and Resolution=1920x1080i

c. Source Test ID 7-9: TMDS – Clock Jitter at 3dB Equalization & 1920x1080i Resolution

OC_S[3:0]	Output	Clock Jitter	Max Spec	Units
0000	CLK+/-	0.103	0.25	T_{BIT}
0101	CLK+/-	0.088	0.25	T_{BIT}

Table 3: Clock Jitter at J304 when EQ=3dB and Resolution=1920x1080i

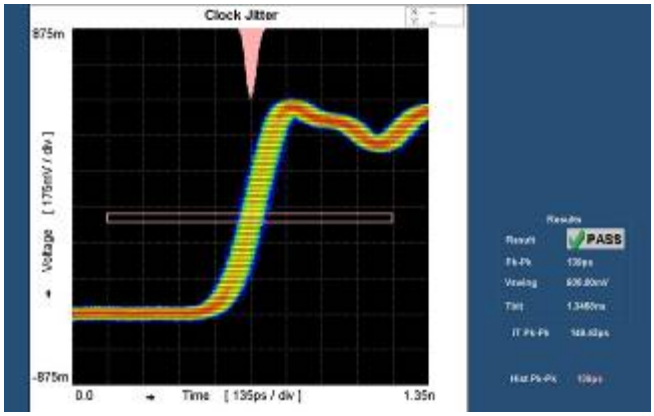


Figure 14: Clock Jitter of CLK when OC_S[3:0]=0000

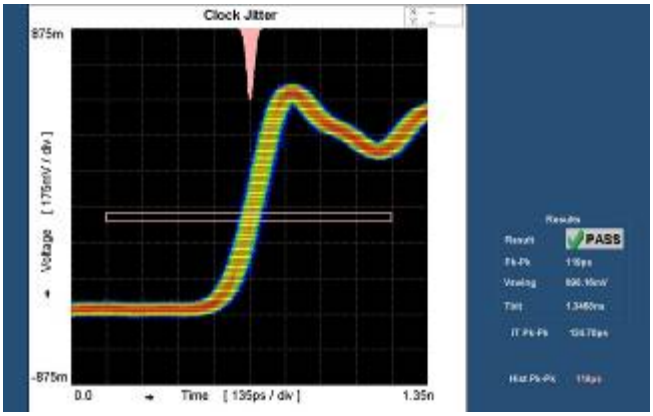


Figure 15: Clock Jitter of CLK when OC_S[3:0]=0101

d. Source Test ID 7-10: TMDS – Data Jitter & Eye Diagrams at 3dB Equalization & 1920x1080i Resolution

OC_S[3:0]	Output	Data Jitter	Max Spec	Units
0000	D2+/-	0.12	0.3	T_{BIT}
0101	D2+/-	0.14	0.3	T_{BIT}

Table 4: Data Jitter at J304 when EQ=3dB and Resolution=1920x1080i

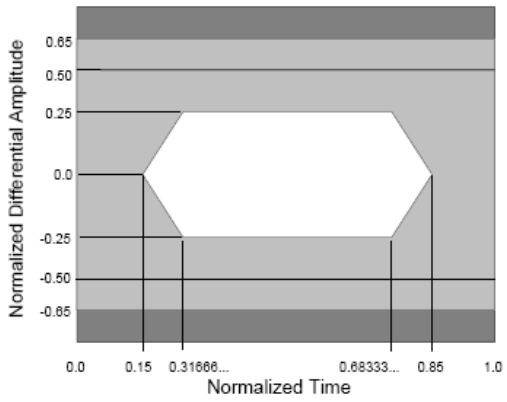


Figure 16: Source Eye Diagram

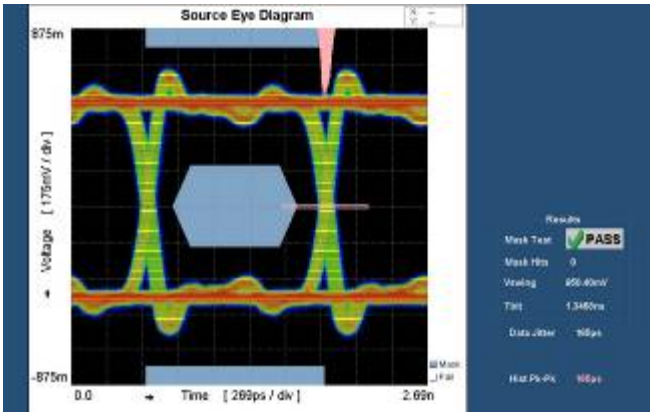


Figure 17: Eye Diagram of D2 when OC_S[3:0]=0000

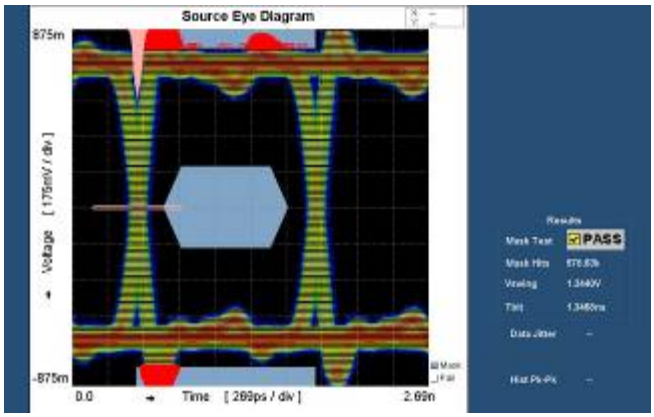


Figure 18: Eye Diagram of D2 when OC_S[3:0]=0001

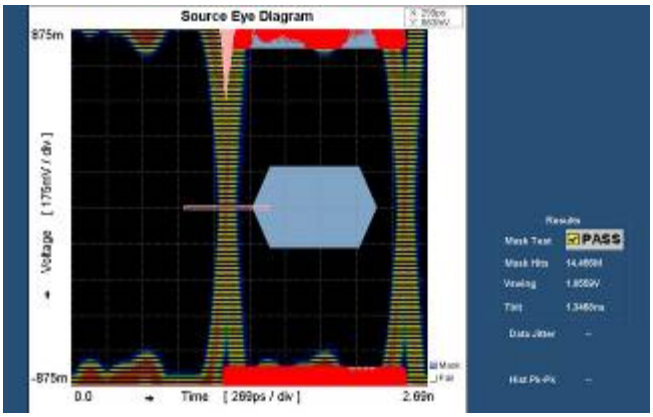


Figure 19: Eye Diagram of D2 when OC_S[3:0]=0010

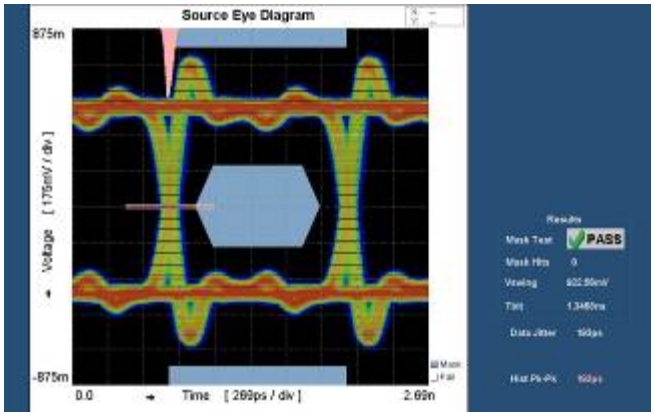


Figure 20: Eye Diagram of D2 when OC_S[3:0]=0101

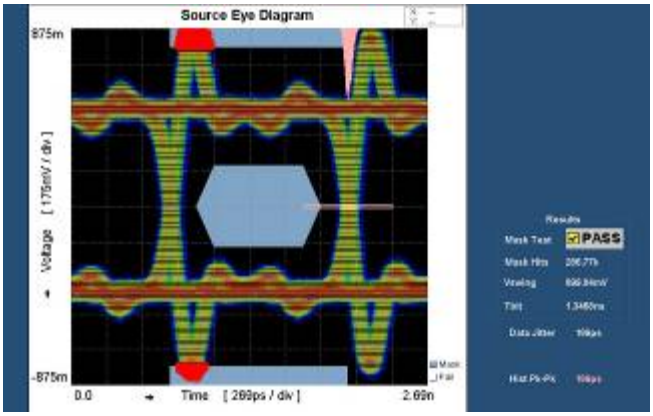


Figure 21: Eye Diagram of D2 when OC_S[3:0]=0110

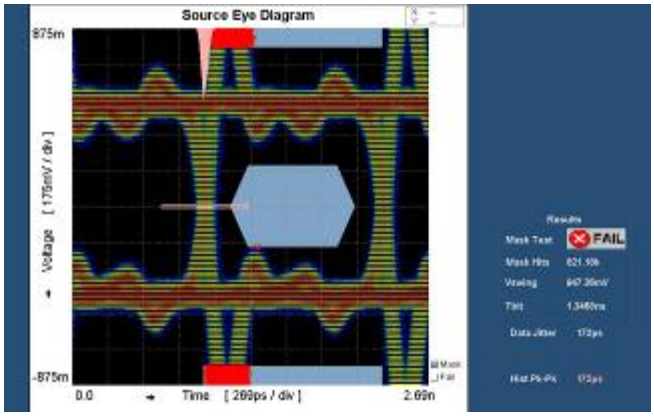


Figure 22: Eye Diagram of D2 when OC_S[3:0]=0111

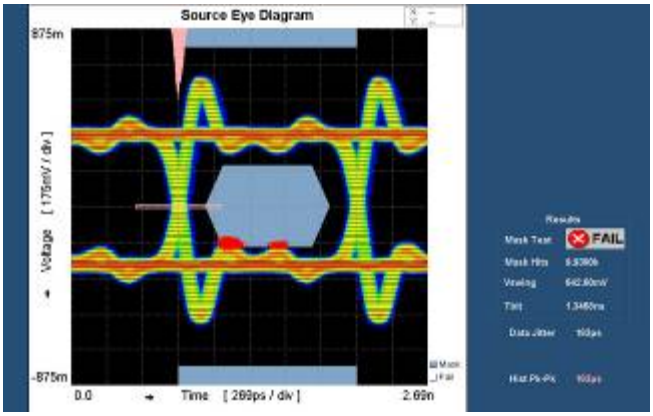


Figure 23: Eye Diagram of D2 when OC_S[3:0]=1001

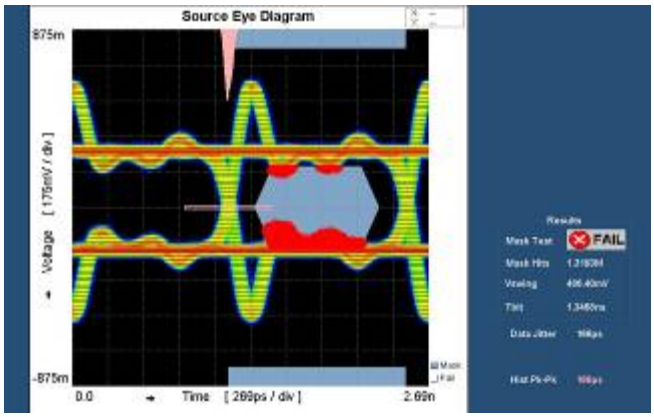


Figure 24: Eye Diagram of D2 when OC_S[3:0]=1010

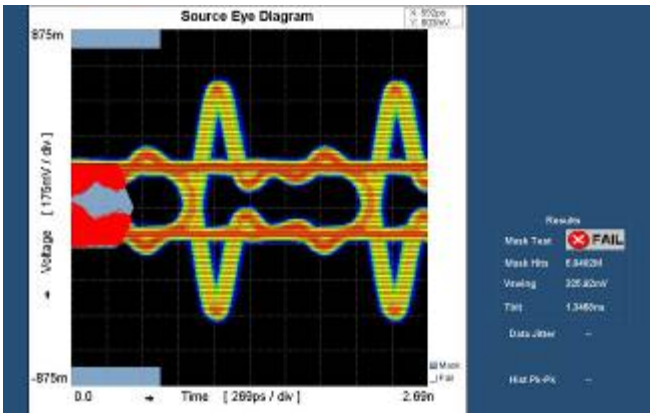


Figure 25: Eye Diagram of D2 when OC_S[3:0]=1011

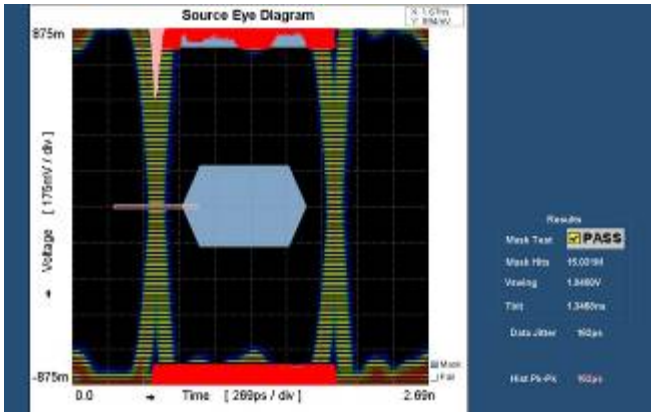


Figure 26: Eye Diagram of D2 when OC_S[3:0]=1100

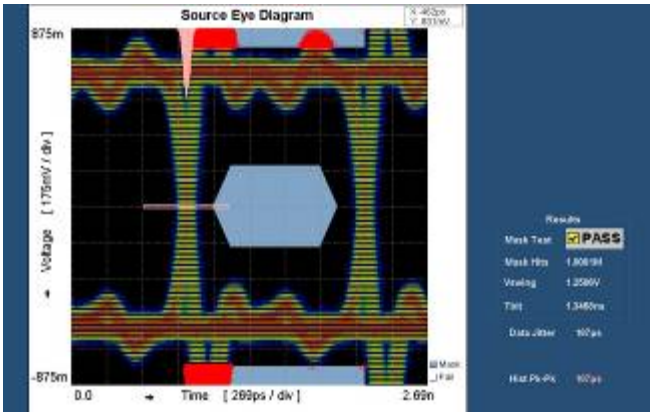


Figure 27: Eye Diagram of D2 when OC_S[3:0]=1101

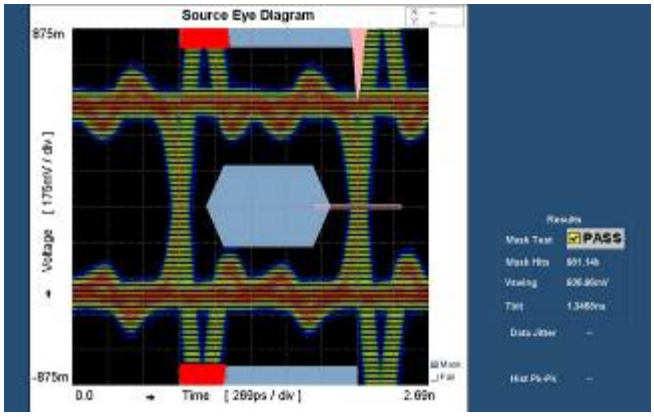


Figure 28: Eye Diagram of D2 when OC_S[3:0]=1110

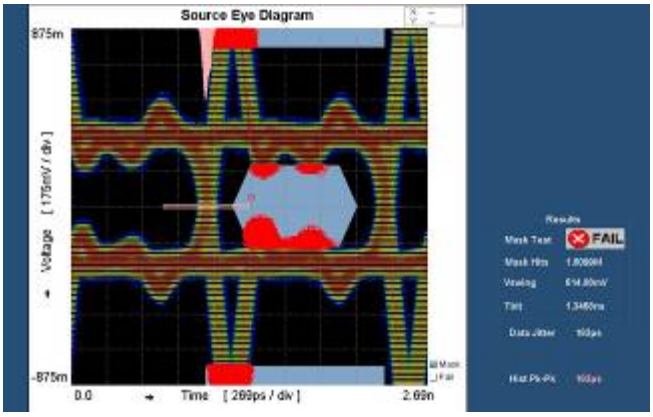


Figure 29: Eye Diagram of D2 when OC_S[3:0]=1111

e. Sink Test ID 8-8: TDR Measurement

Differential impedance of PI3HDMI301 on an HDMI-HDMI demo board is measured to confirm the trace impedance is within the requirement described in Test ID 8-8 in HDMI Compliance Test Specification Version 1.3a.

Test ID 8-8: TMDS – Differential Impedance

Reference	Requirement
[HDMI: Table 4-20] HDMI Sink Impedance at TP2	Through-connection impedance : 100Ω ± 15%* ** A single excursion is permitted out to a max/min of 100 ohms ±25% and of a duration less than 250psecs.* At Termination impedance (when Vicm is within Vicm1 range) 100 ohms ±10%

Table 5: HDMI Pre-test Test ID 8-8 Specification

CDF field Sink_Diff_PowerOn = N for each high speed signal input. At-termination impedance can be measured without powering up PI3HDMI301. The termination of each clock is switched from 50Ω to 250kΩ pull-up when PI3HDMI301 is not powered up. Thus, at-termination impedance cannot be obtained at clock signal.

Through impedance is measured at input side of the demo board. Filter of 180ps is employed throughout the following measurement.
Sink_Term_Distance of CLK at Port A = 0.52ns
Sink_Term_Distance of CLK at Port B = 0.42ns
Sink_Term_Distance of CLK at Port C = 0.58ns

Through Impedance		D2	D1	D0	CLK	Spec		Units
						Min	Max	
Port A	**Min**	93	93	93	95	85	115	Ω
	Max	105	101	103	105	85	115	Ω
Port B	**Min**	94	94	93	94	85	115	Ω
	Max	106	103	104	102	85	115	Ω
Port C	**Min**	93	93	93	95	85	115	Ω
	Max	106	103	105	103	85	115	Ω

Table 6: Through Impedance Result

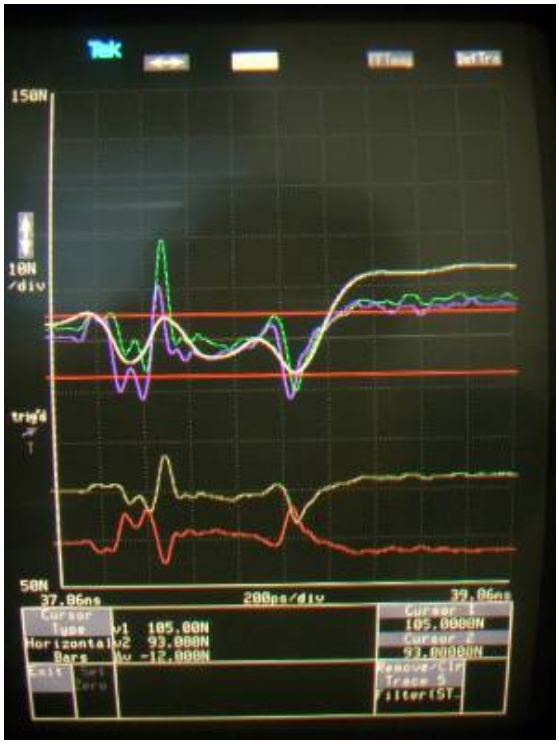


Figure 30a: Through Impedance of D2 at Port A

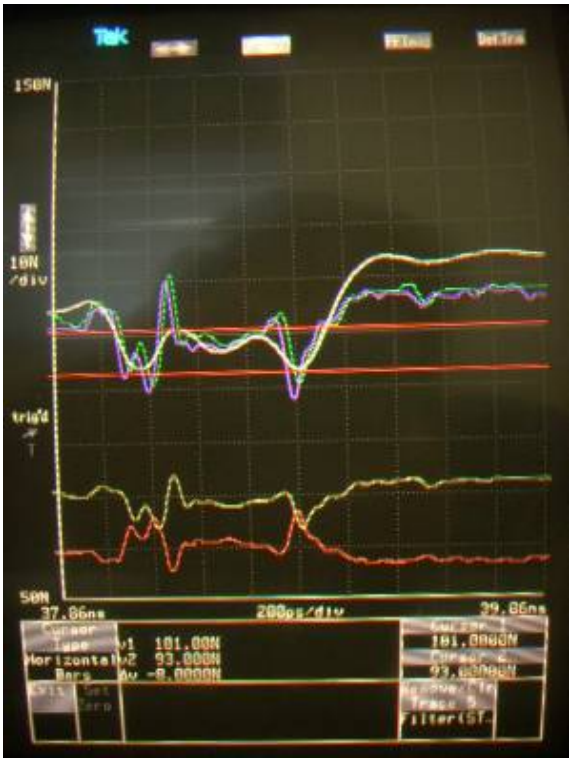


Figure 30b: Through Impedance of D1 at Port A

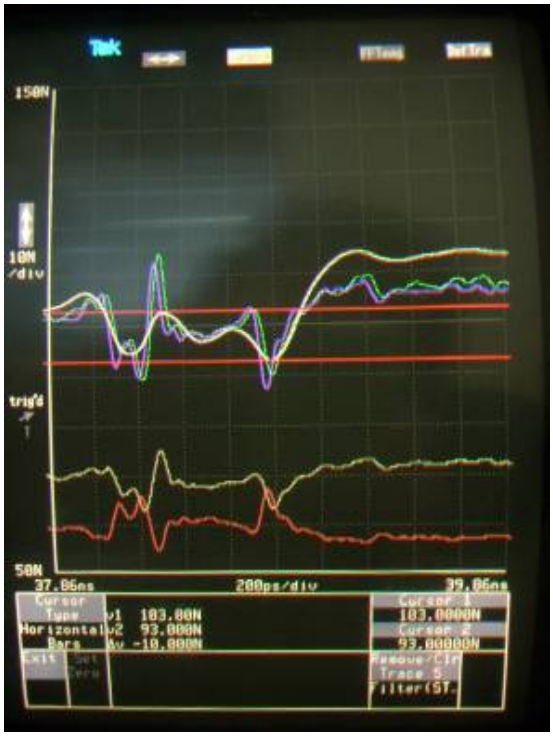


Figure 30c: Through Impedance of D0 at Port A

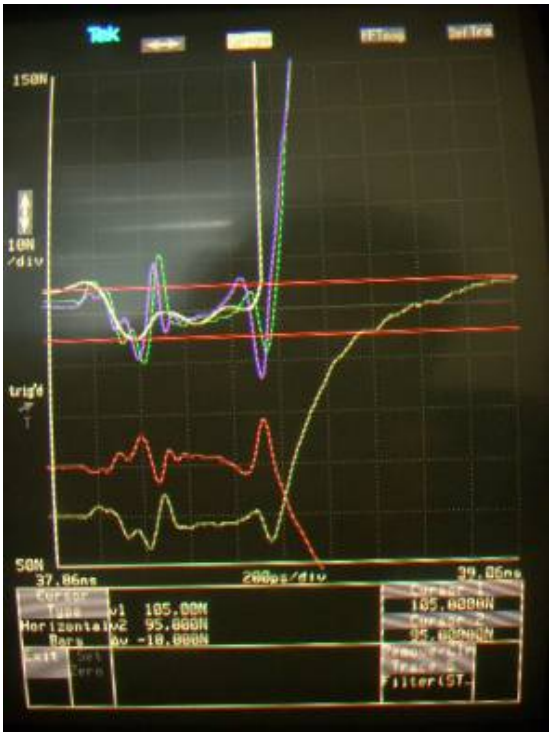


Figure 30d: Through Impedance of CLK at Port A

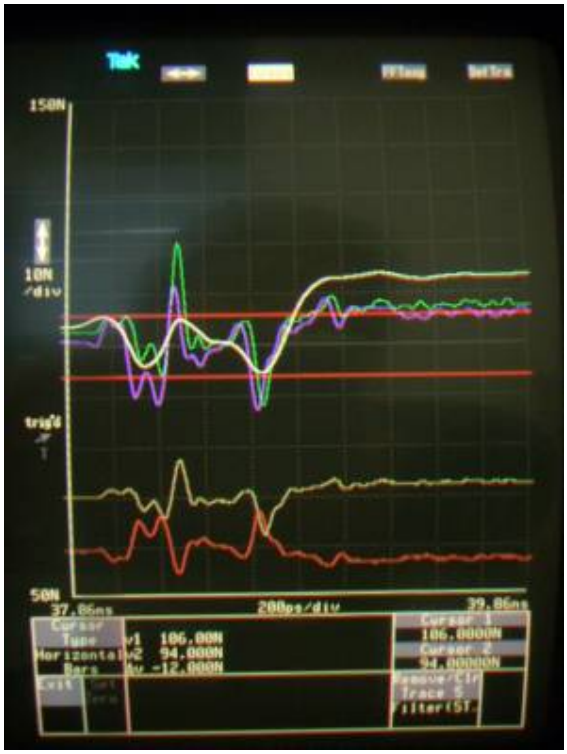


Figure 31a: Through Impedance of D2 at Port B

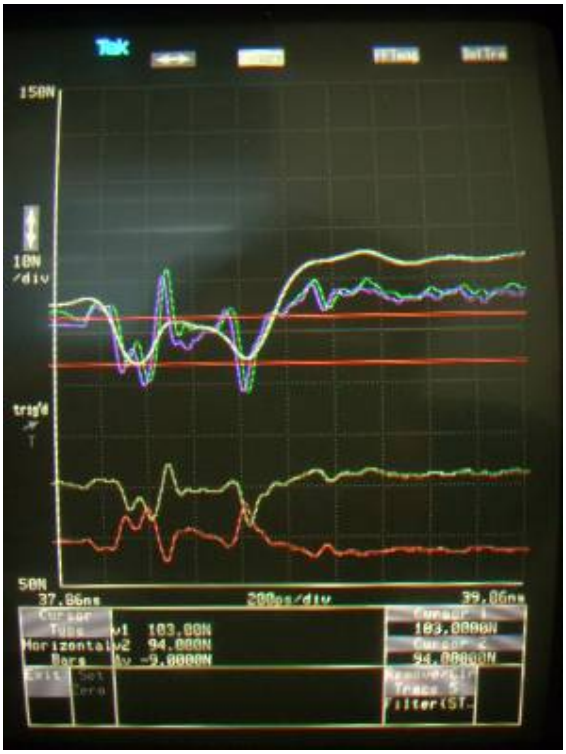


Figure 31b: Through Impedance of D1 at Port B

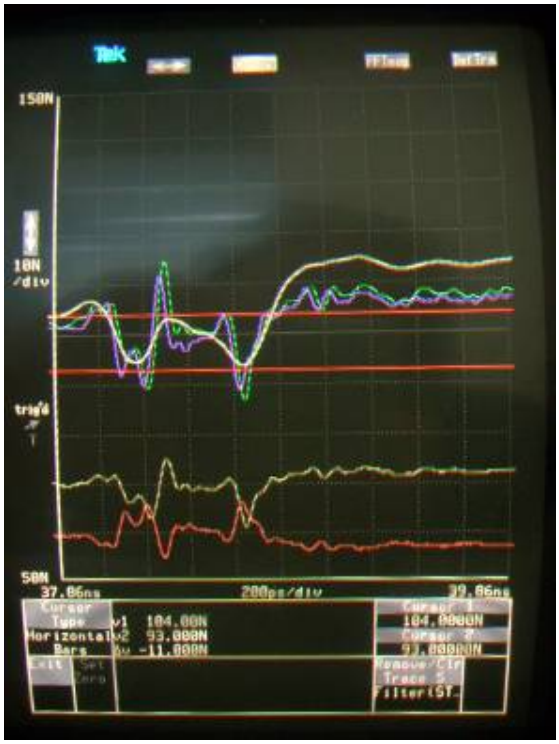


Figure 31c: Through Impedance of D0 at Port B

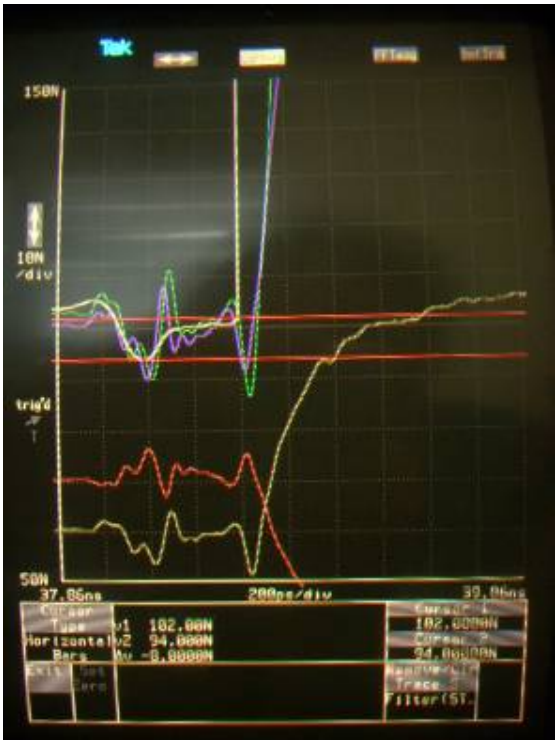


Figure 31d: Through Impedance of CLK at Port B

Figure 32a: Through Impedance of D2 at Port C

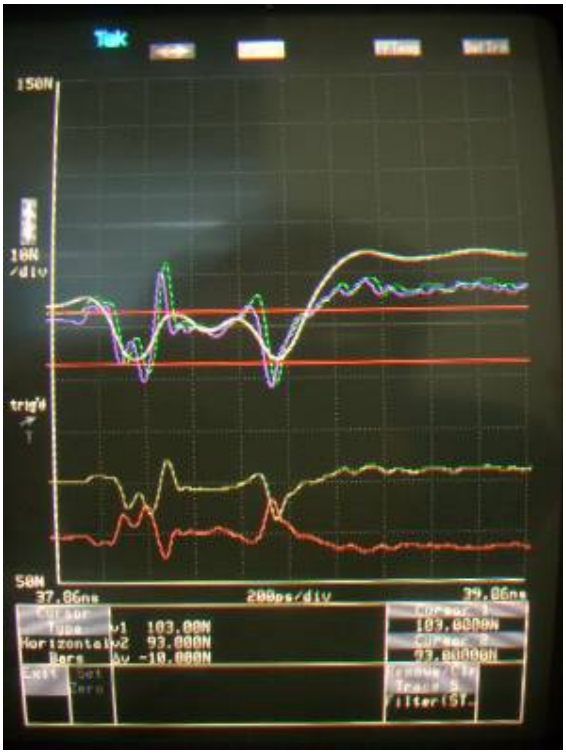


Figure 32b: Through Impedance of D1 at Port C

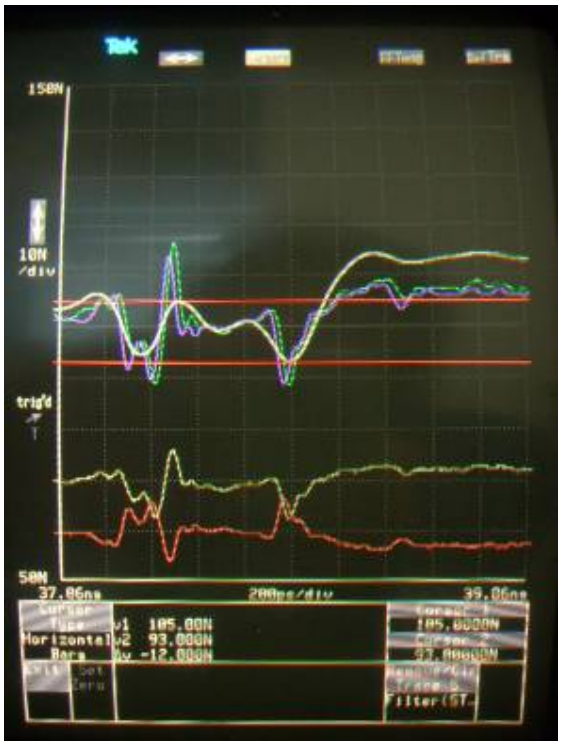


Figure 32c: Through Impedance of D0 at Port C

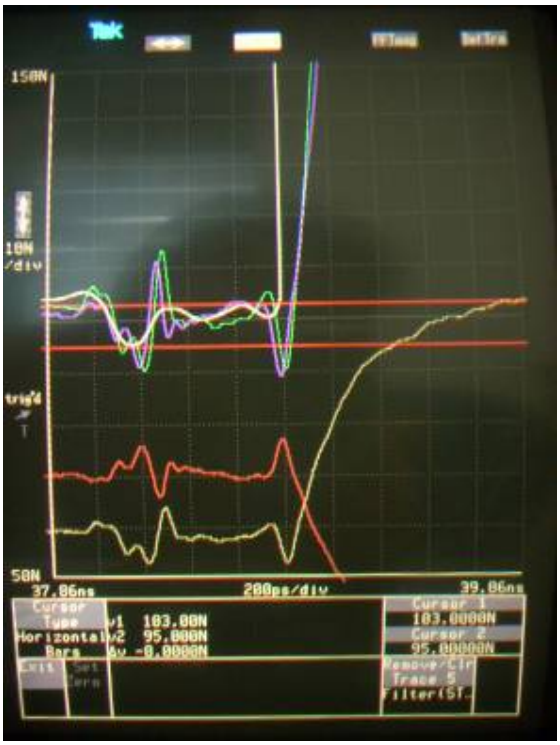


Figure 32d: Through Impedance of CLK at Port C

f. Sink Test ID 8-9: DDC/CEC Line Capacitance Measurement

The capacitances of SDA and SCL signals which go through EEPROM AT24C02B are tested. The capacitance of CEC line connecting input to output HDMI is also measured. Results below show that the capacitances are within HDMI CTS V1.3a requirement.

C_{DUT} = C2 – C1
Setting of Impedance Analyzer for measuring capacitance:
For SDA/SCL, Freq=100kHz, DC Bias=2.5V, Power=15dBm (AC~1.8Vpp at DUT), IF BW=1kHz, Sweep Time=1s
For CEC, Freq=100kHz, DC Bias=1.65V, Power=15dBm (AC~1.8Vpp at DUT), IF BW=1kHz, Sweep Time=1s

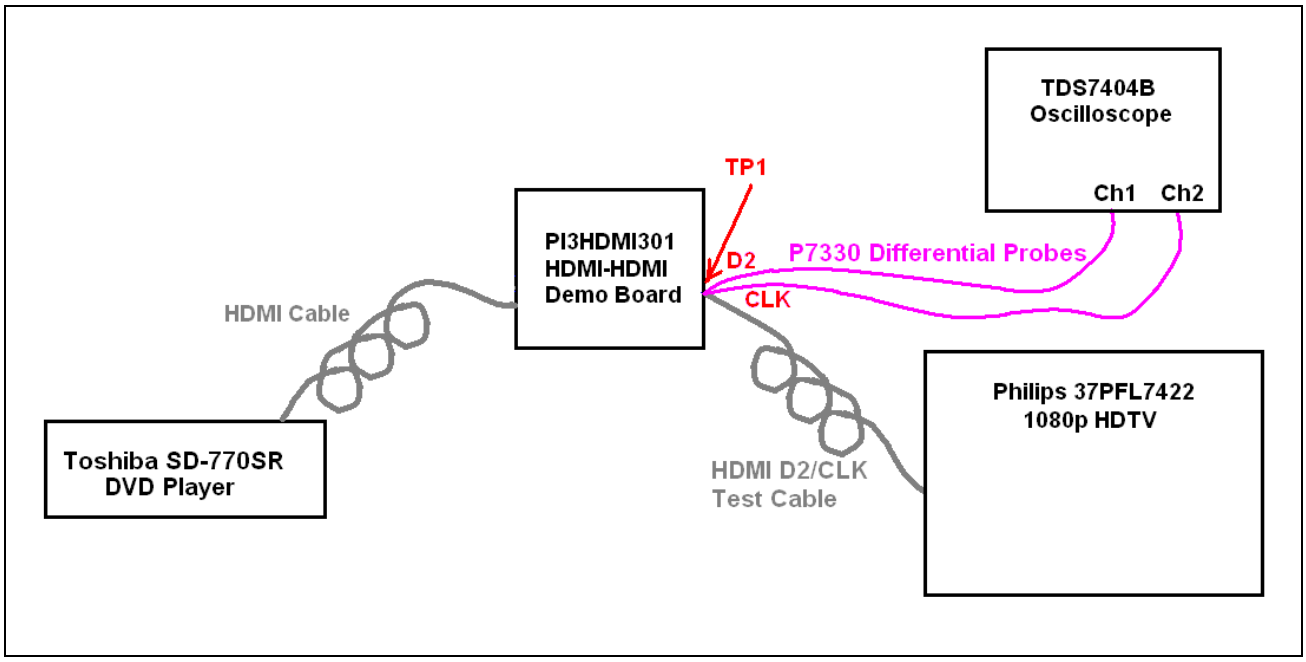
Pin	Parameter	DUT Power		Spec		Units
		Off	On	Min	Max	
SDA	C1	6.9	6.9	NA	NA	pF
	C2	17.4	21.3	NA	NA	pF
	C_{DUT}	10.5	14.4		50	pF
SCL	C1	6.9	6.9	NA	NA	pF
	C2	16.2	20.0	NA	NA	pF
	C_{DUT}	9.3	13.1		50	pF
CEC	C1	7.0	7.0	NA	NA	pF
	C2	24.7	24.8	NA	NA	pF
	C_{DUT}	17.7	17.8		200	pF

Table 7: DDC/CEC Line Capacitance Result at Connector J301

Appendix A: Test Setup

Test setup:

a. For Source Test



Equipment Use:

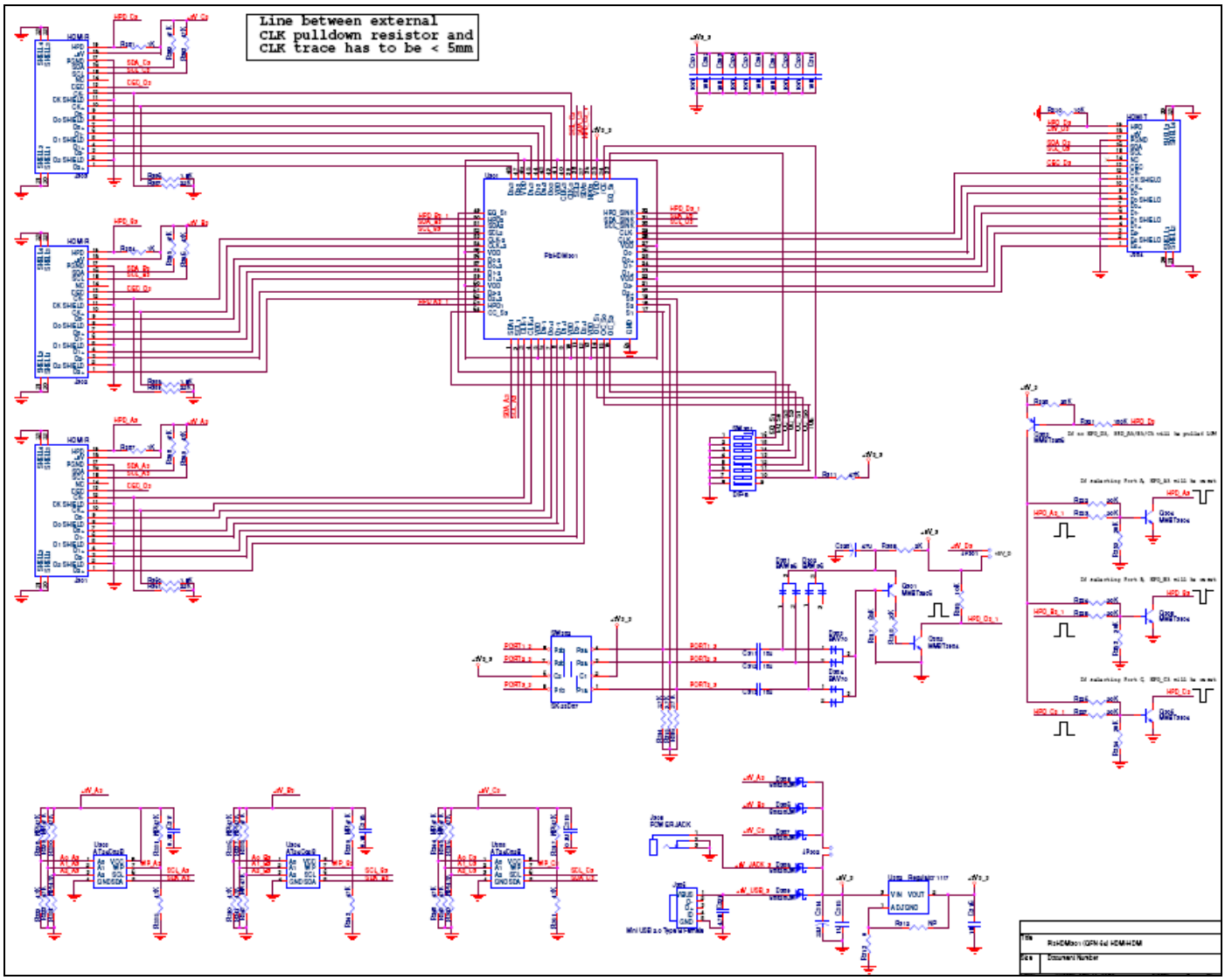
a. For Source Test

- TDS7404B Oscilloscope with P7330 Differential Probes
- 1-meter HDMI Cable
- 1-meter HDMI D2/CLK Test Cable
- Toshiba SD-770SR DVD Player
- Philips 37PFL7422 HDTV
- Agilent Power Supply
- 5V DC Adaptor

b. For Sink Test

- Tek11801C Digital Sampling Oscilloscope
- Agilent 4395A Impedance Analyzer with 43961A and 16092A
- SMA Matching Cables
- PSC High BW TDR Test Fixture
- PSC High BW Cap Test Fixture
- Agilent Power Supply
- 5V DC Adaptor

Appendix B: PCB Schematic



Appendix C: PCB Layout Requirements

a. Stack Up:

Plane	Material	Thickness (mil)
W		
Signal		1.9
Prepreg	1080 + 2116	7.3
Ground		1.2
Core		44
Power		1.2
Prepreg	1080 + 2116	7.3
Signal		1.9

b. Isolation Spacing = 30 mil

c. Width & Spacing (W/S) of 100Ω Differential Trace = 9.0 / 10 mil
* W/S for 80 mils before and after contacting the TMDS input/output pads of PI3HDMI301 = 5.0 / 15 mil to compensate the impedance drop of PI3HDMI301 solder pads

Appendix D: BOM List

Item	Quantity	Reference	Description
1	10	C301, C302, C303, C304, C305, C306, C307, C308, C309, C310	10nF Capacitor
2	1	C314	22uF Capacitor
3	2	C315, C316	1uF Capacitor
4	3	C317, C318, C319	0.1uF Capacitor
5	1	C320	4.7uF Capacitor
6	3	C311, C312, C313	10uF Capacitor
7	1	C320	47uF Capacitor
8	2	D301, D302	BAW56 Common Anode Double Diode
9	2	D303, D304	BAV70 Common Cathode Double Diode
10	5	D305, D306, D307, D308, D309	B0520LW Schottky Rectifier
11	2	JP301, JP302	2-pin Header
12	3	J301, J302, J303	HDMI Receptacle Connector
13	1	J304	HDMI Plug Connector
14	1	J305	Power Jack
15	1	J306	Mini USB Female Connector
16	2	Q301, Q303	MMBT3906 PNP Transistor
17	4	Q302, Q304, Q305, Q306	MMBT3904 NPN Transistor
18	3	R301, R304, R307	1kΩ Resistor
19	19	R302, R303, R305, R306, R308, R309, R311, R330, R332, R333, R335, R338, R340, R341, R343, R346, R348, R349, R351	47kΩ Resistor
20	2	R310, R319	10kΩ Resistor
21	1	R313	0Ω Resistor
22	3	R314, R315, R316	2.7kΩ Resistor
23	1	R317	68kΩ Resistor
24	11	R318, R320, R322, R323, R324, R325, R326, R327, R352, R353, R354	20kΩ Resistor
25	1	R321	100kΩ Resistor
26	1	R355	2kΩ Resistor
27	3	R356, R358, R360	1.5kΩ Resistor
28	3	R357, R359, R361	22kΩ Resistor
29	12	R328, R329, R331, R334, R336, R337, R339, R342, R344, R345, R347, R350	NOT CONNECTED
30	1	SW301	DIP-8 Switch
31	1	SW302	DP3T Switch
32	1	U301	PI3HDMI301 HDMI Switch
33	1	U302	1117 Regulator
34	2	U303, U304, U305	AT24C02B EEPROM